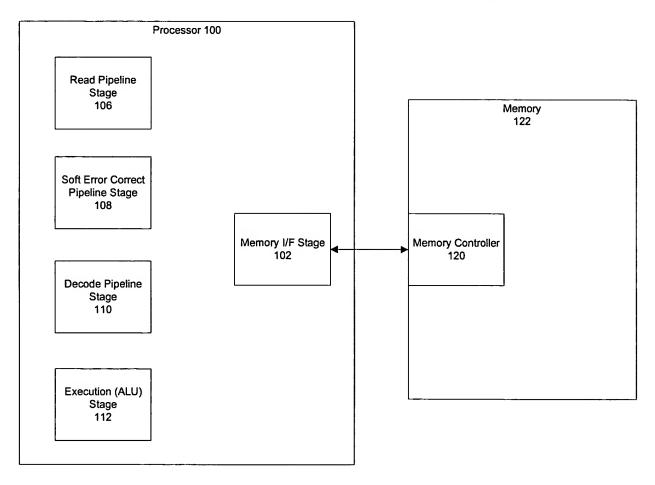
and the second of the second of

Figure 1



T₀ T₂ **T**₃ **T**₄ T₅ T₆ T₇ T₁ DR1 206 EX1 210 IR1 IC1/ID1 AA1 DC1 200 202 204 208 AA2 224 IC2/ID2 DR2 EX2 230 IR2 DC2 220 222 226 228 IR3 230 IC3/ID3 AA3 234 DR3 DC3 EX3 232 236 238 240

Figure 2

T ₀	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	T ₇	T ₈
IR1 300	IC1 (start) 302	IC1 (cont.) 304	WC1 (dummy) 306	EX1 308				
		IR2 310	IC2 (start) 312	IC2 (cont.) 314	WC2 (dummy) 316	EX2 318		
				IR3 320	IC3 (start) 322	IC3 (cont.) 324	WC3 (dummy) 326	EX3 328

Figure 3

Start READ Stage for Next Requested Address 400 Retrieve Requested Data (e.g., 32 bits) and ECC (e.g., 6 bit Hamming Code) 402 No Correction Pass Data to Stage Enabled? **Utilization Stage** 404 406 Yes Pass Retrieved Information to Correction Stage 408 Next Cycle Await Next Memory Cycle

Figure 4

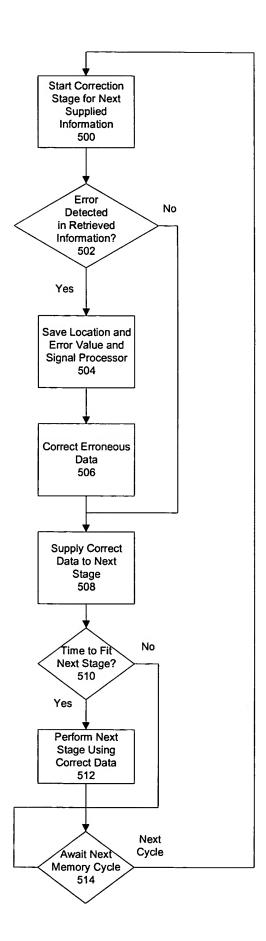


Figure 5

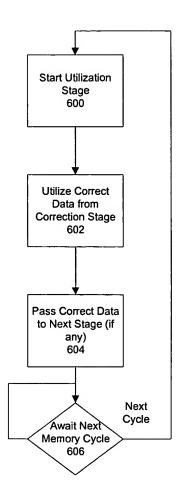


Figure 6

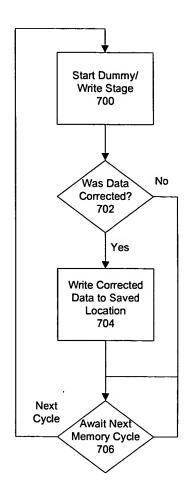


Figure 7